ABSTRACT

When a voltage oscillator oscillates abnormally and a PLL circuit stops operating, in order to return to normal operation quickly, presence/absence of a comparison signal (fc) outputted from a frequency divider (4) is detected, and at times when there is no comparison signal (fc), an output signal of a phase comparator (4) is forcibly controlled to a low level temporarily, and an oscillation frequency of a voltage control oscillator (3) is decreased. The present invention is suitable for generation of a sampling clock of a wide range which is used when digitally processing analog image signals, and for the like.